IN THE CLAIMS

The current claims are presented:

1. (Previously Presented) A wireless receiver system comprising:

a receiver circuit that receives a wireless signal;

a demodulator coupled to the receiver circuit, the demodulator recovering a data signal and at least one clock signal from at least one signal output by the receiver circuit;

a computer configured to generate a read signal; and

a first-in first-out memory coupled to the demodulator to receive the data signal and the at least one clock signal, wherein the first-in first-out memory stores the data signal in response to the at lest one clock signal, and wherein the first-in first-out memory is coupled to the computer to receive the read signal;

wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

2. (Previously Presented) The wireless receiver system of the claim 1 wherein the read signal is synchronized with a computer clock signal.

3. (Canceled)

4. (Previously Presented) The wireless receiver system of claim 1 wherein the computer operates at a higher speed than the at least one clock signal.

5. (Previously Presented) The wireless receiver system of claim 5 wherein the computer reads the data signal from the first-in first-out memory in bursts.

6. (Previously Presented) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

7. (Previously Presented) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

8. (Previously Presented) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

9 – 13. (Canceled)

14. (Previously Presented) A method for receiving data comprising:

receiving a wireless signal;

recovering a data signal and at least one clock signal from the received wireless signal; and

storing the data signal into a first-in first-out memory in response to the at least one clock signal; and

providing, by a computer, a read signal to the first-in first-out memory;

wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

15. (Previously Presented) The method of claim 14 wherein the read signal is synchronized with a computer clock signal.

16. (Canceled)

17. (Previously Presented) The method of claim 14 wherein the computer operates at a higher speed than the at least one clock signal.

18. (Previously Presented) The method of claim 14 wherein the computer reads the data signal from the first-in first-out memory in bursts.

19. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

20. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

21. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

22-41. (Canceled)